

Fig. 1

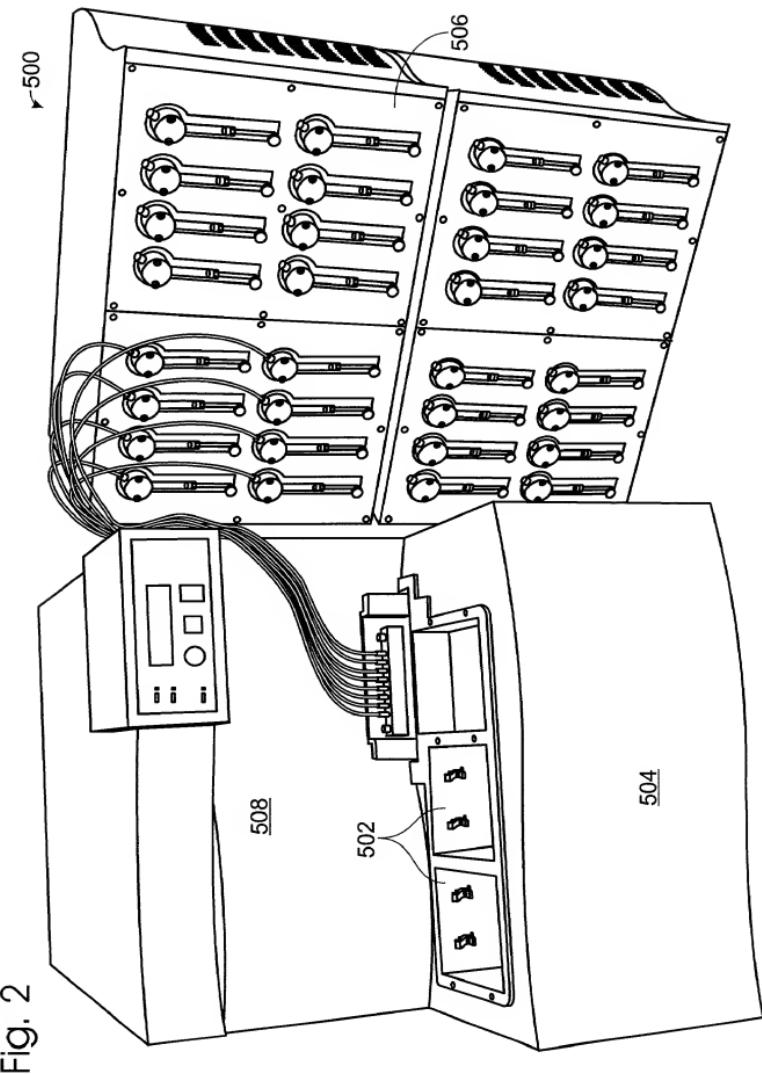


Fig. 3

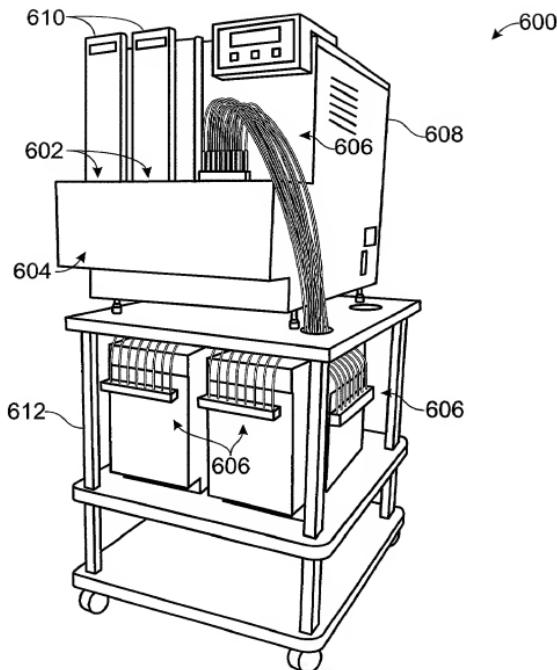
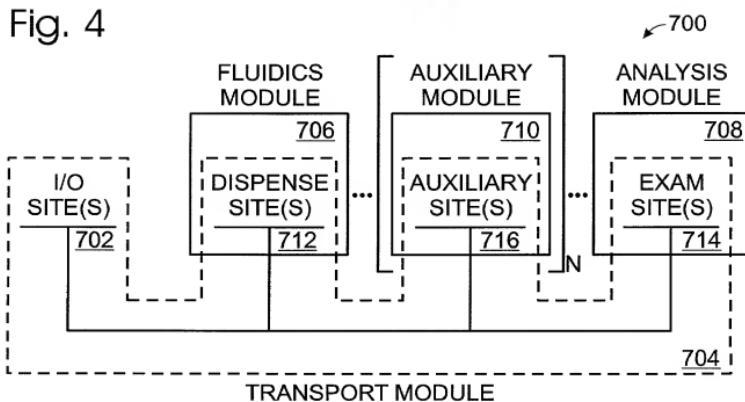
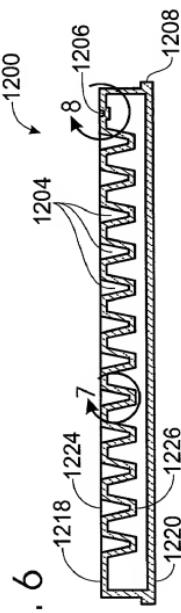
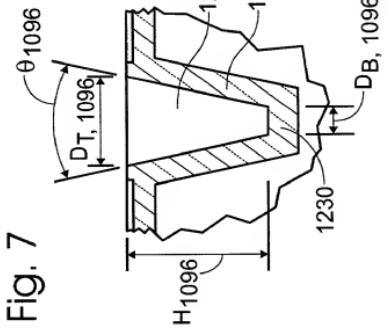
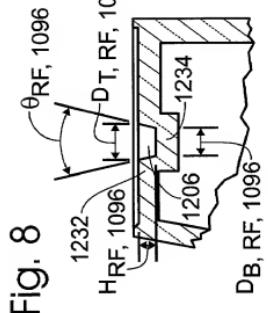
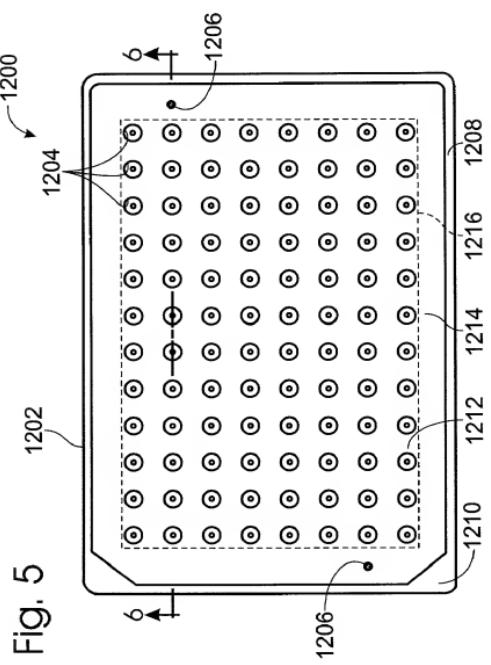


Fig. 4





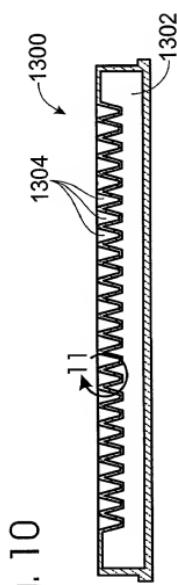
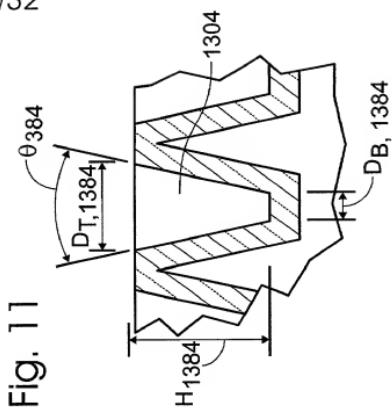
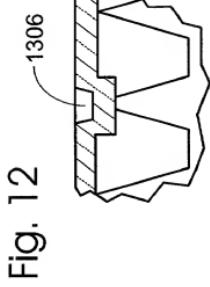
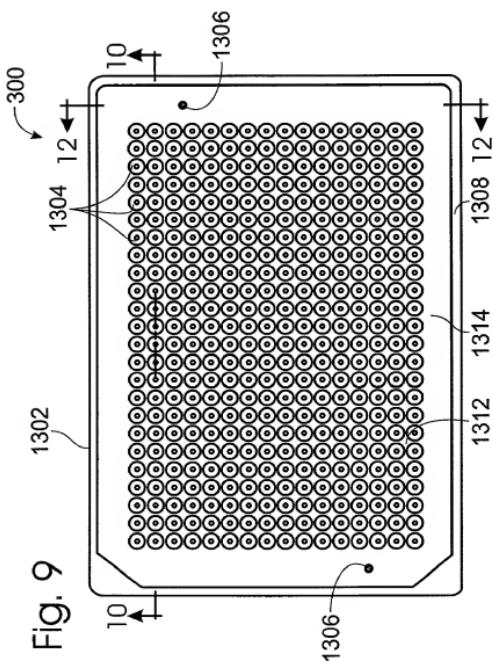


Fig. 13

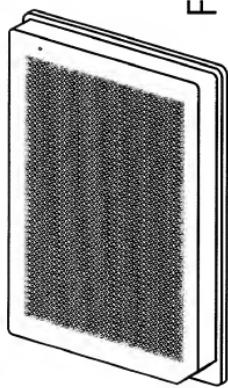


Fig. 14

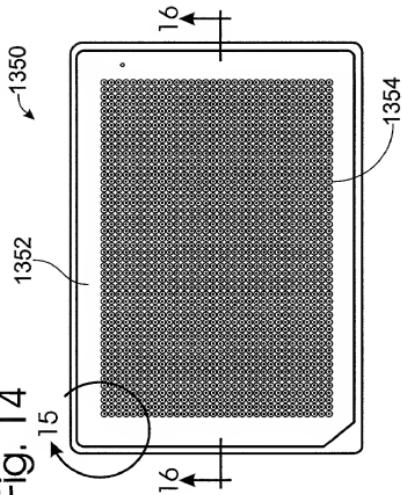


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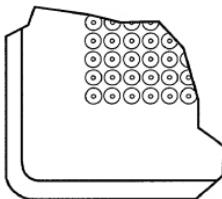


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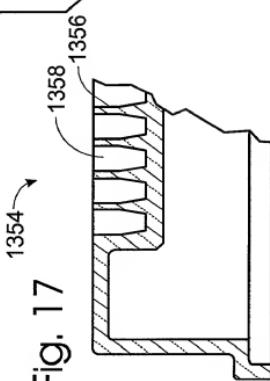
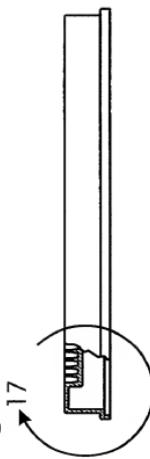


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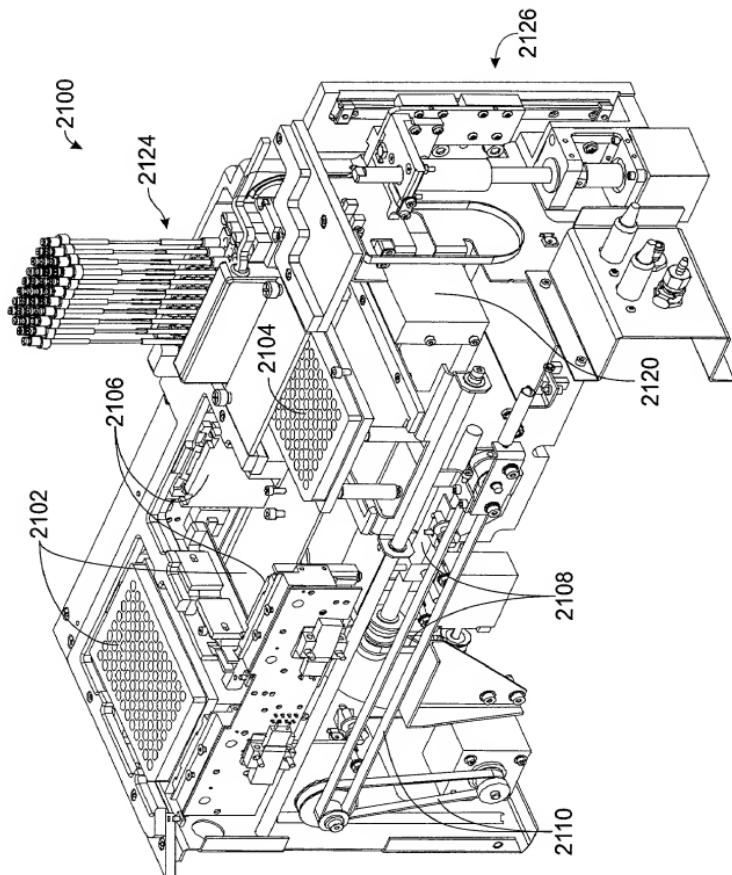


Fig. 18

Fig. 19

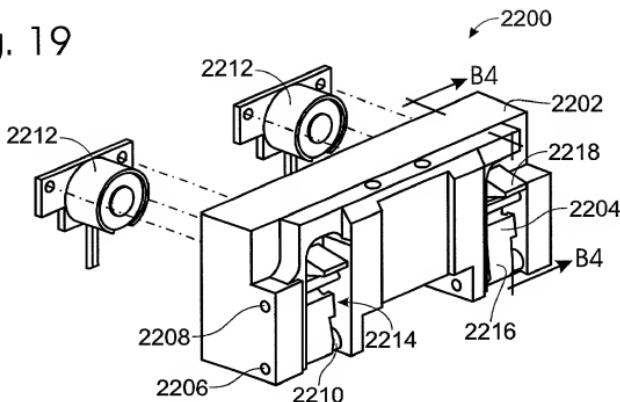


Fig. 20

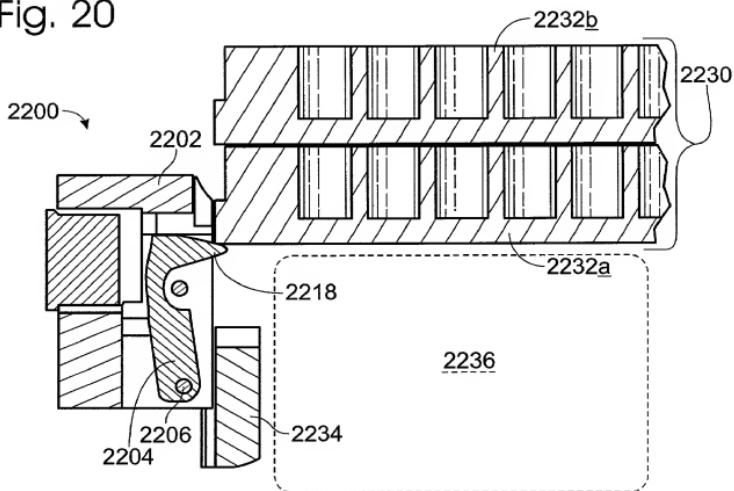


Fig. 21 (INPUT CYCLE)

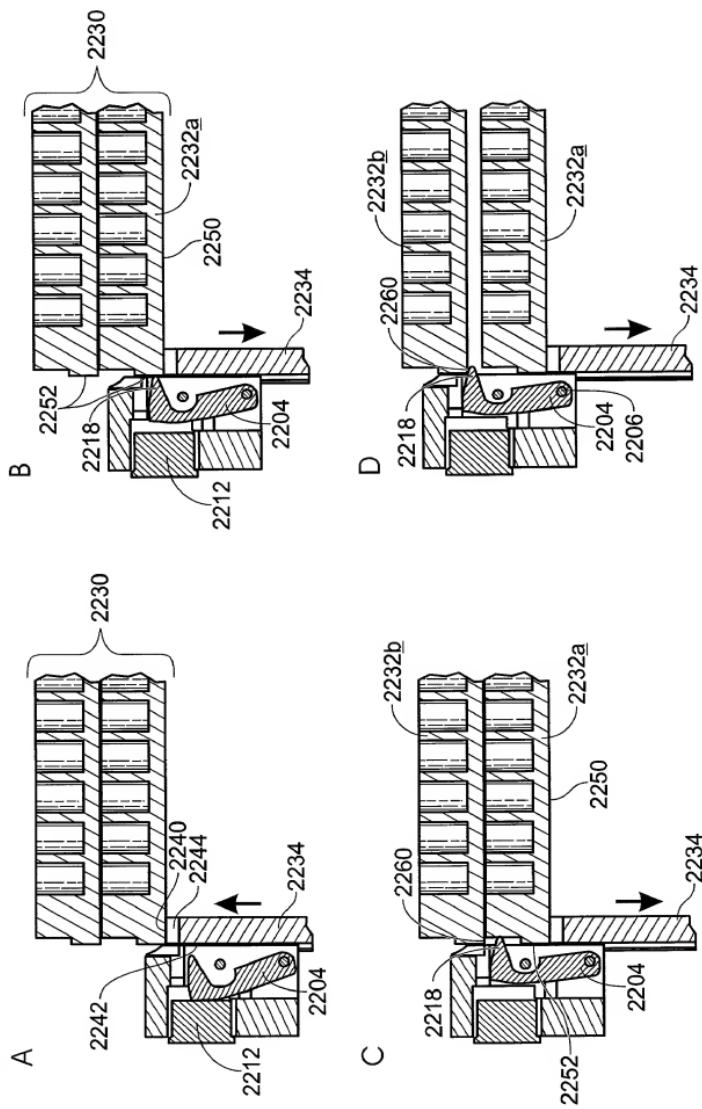


Fig. 22 (OUTPUT CYCLE)

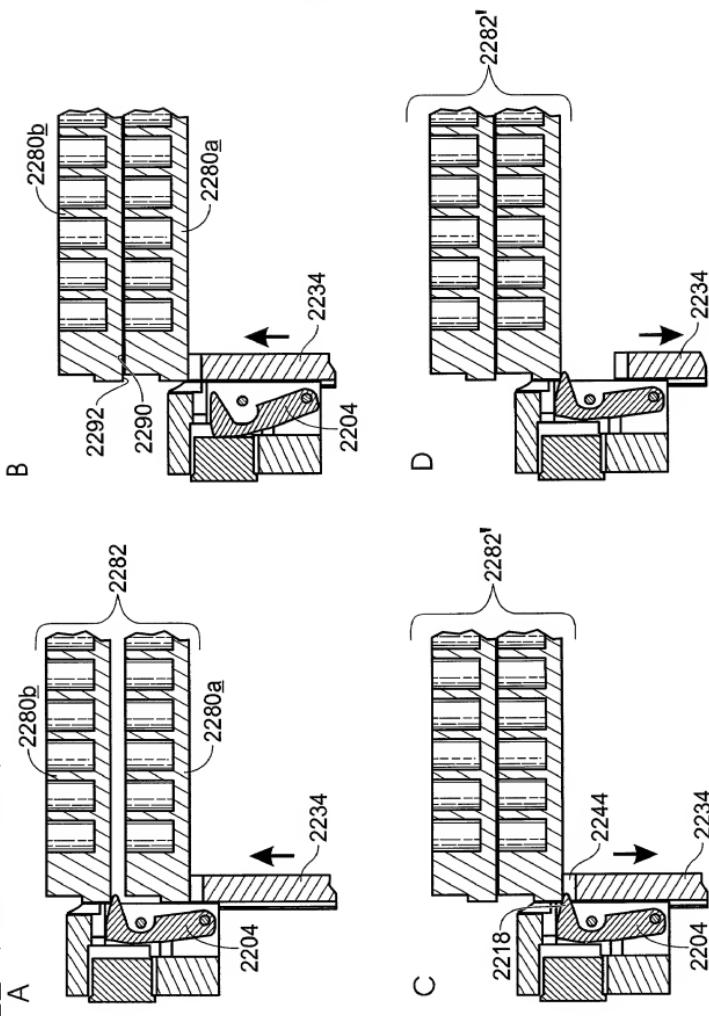
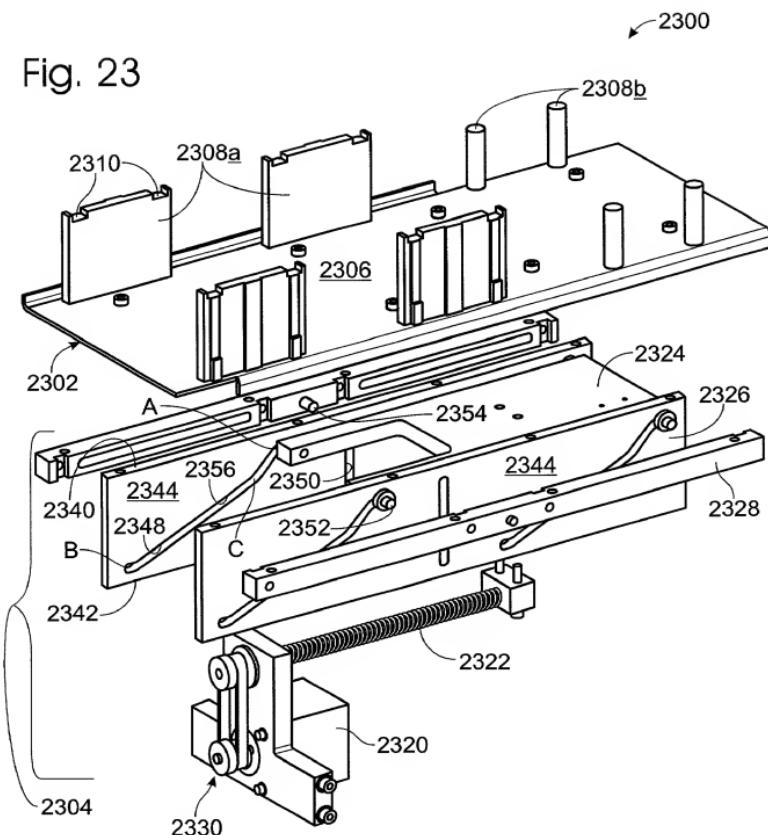


Fig. 23



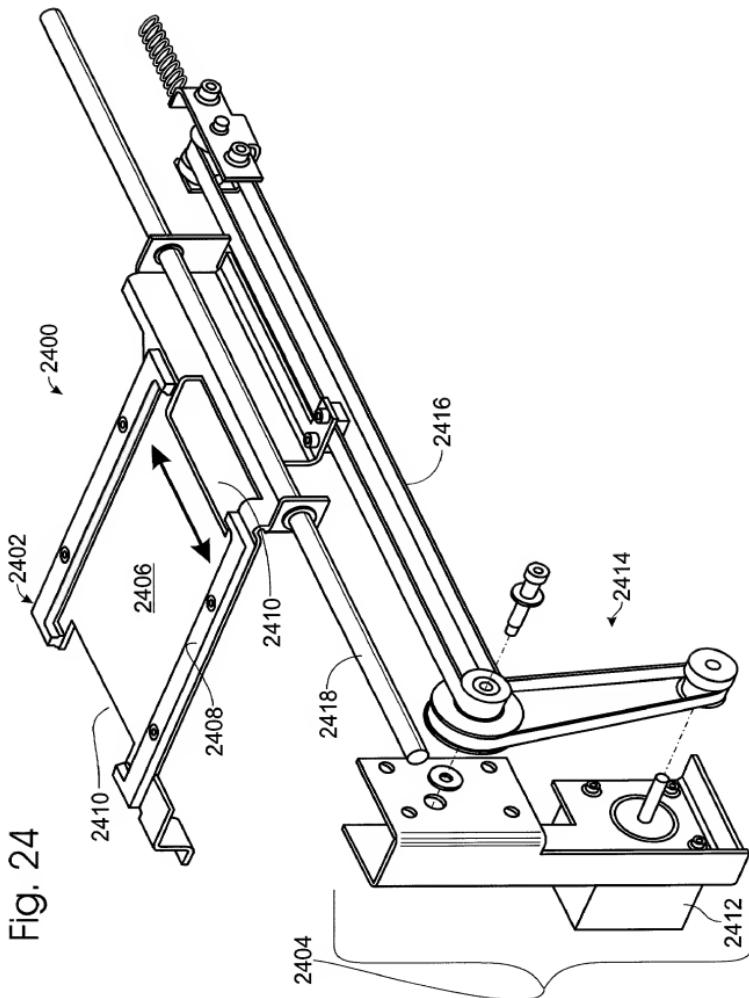


Fig. 25

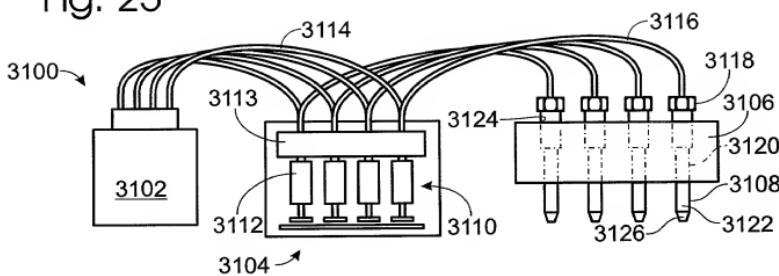


Fig. 26

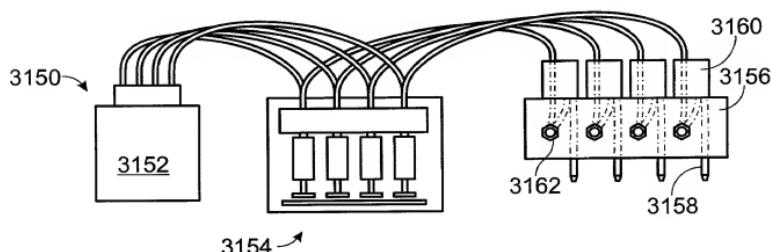


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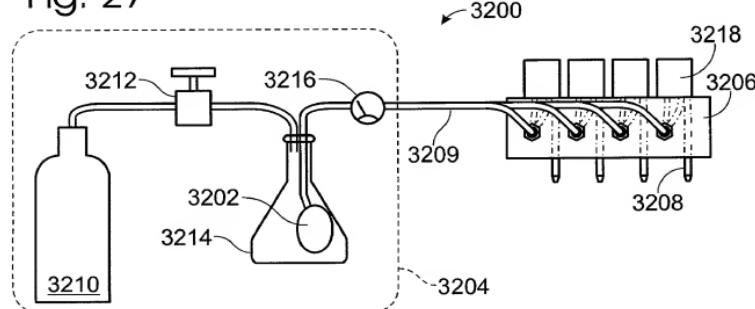


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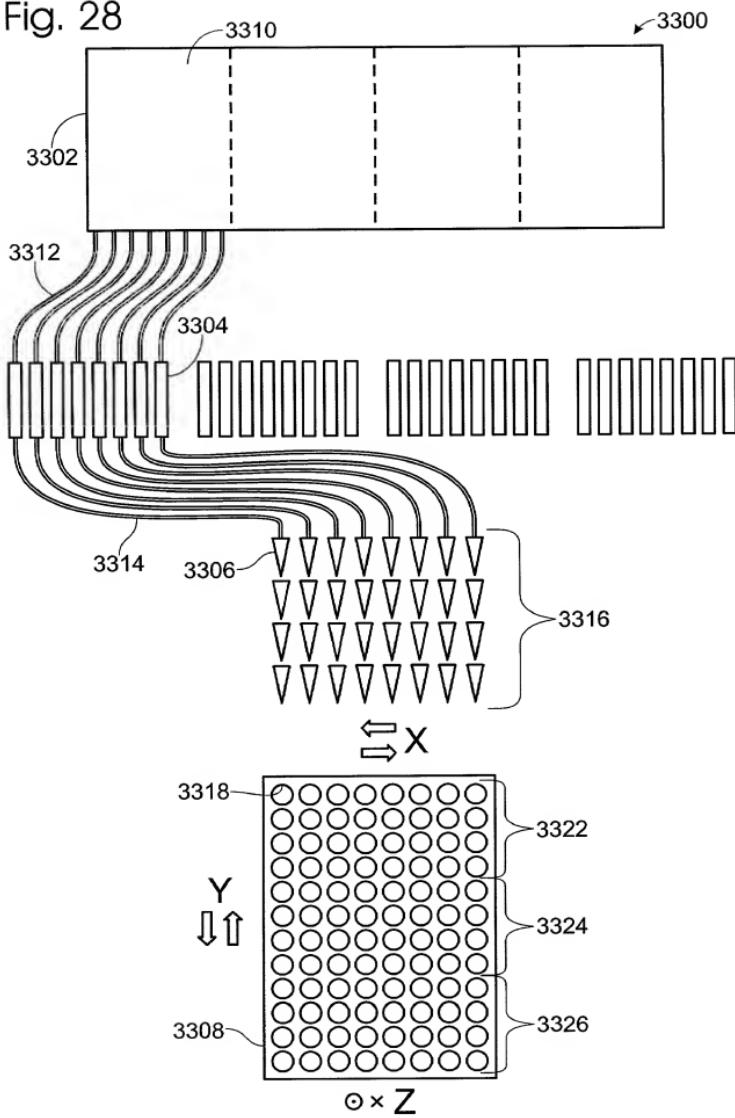


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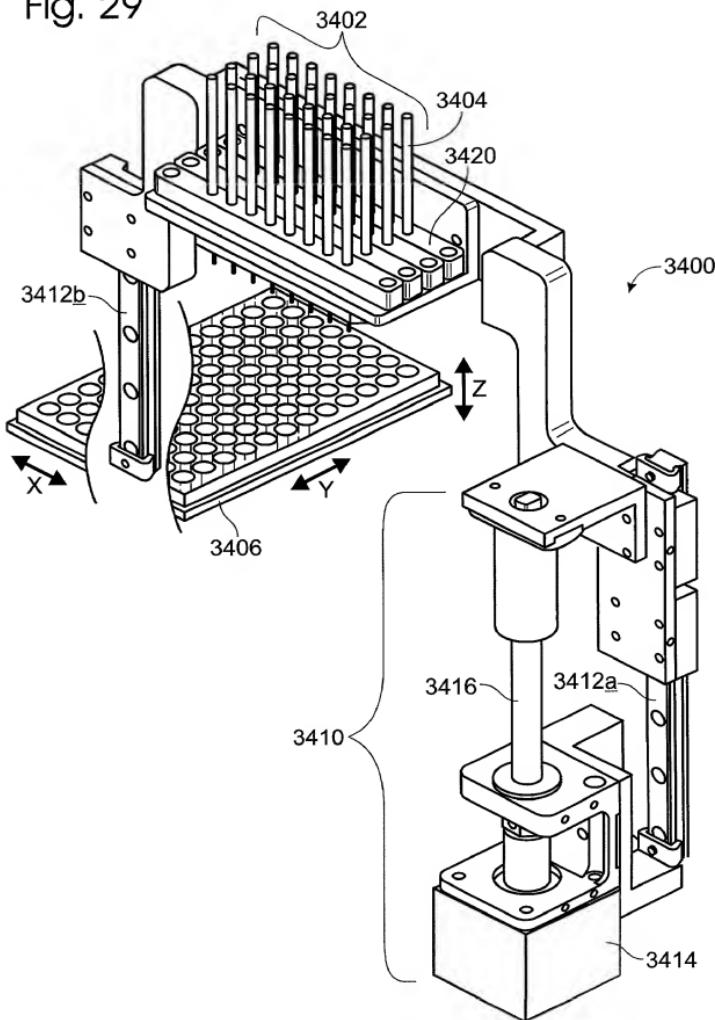


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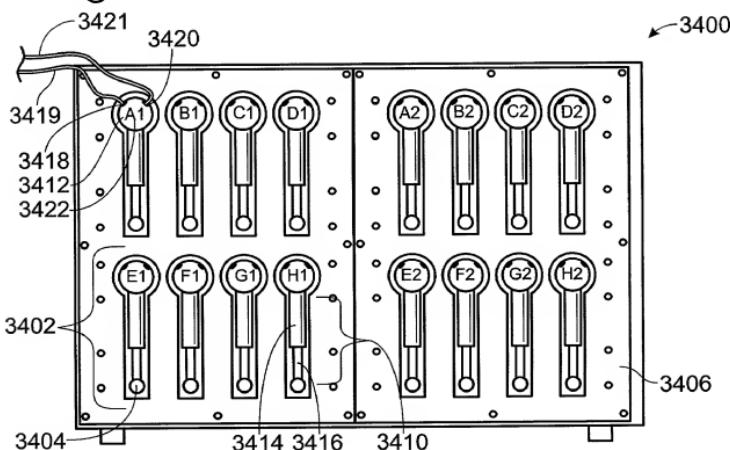


Fig. 31

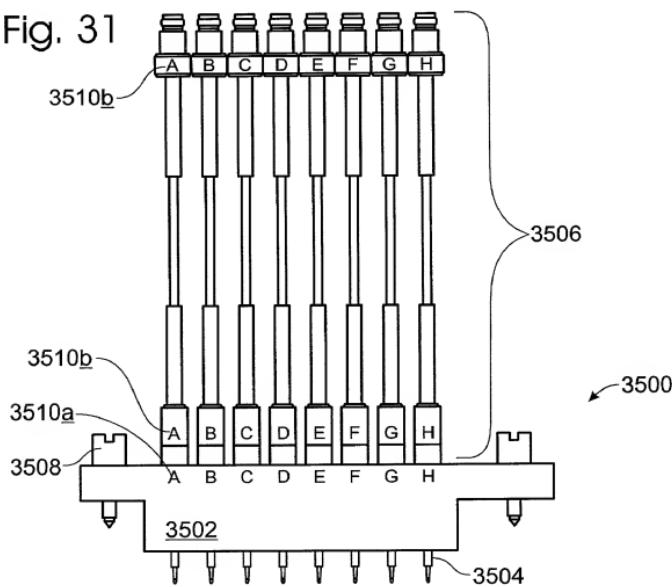


Fig. 32

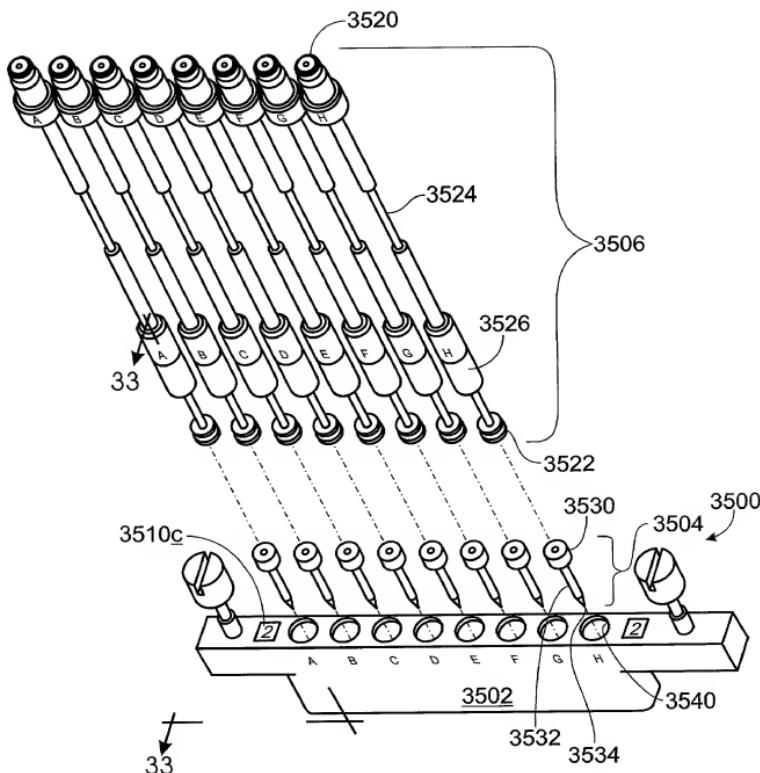


Fig. 33

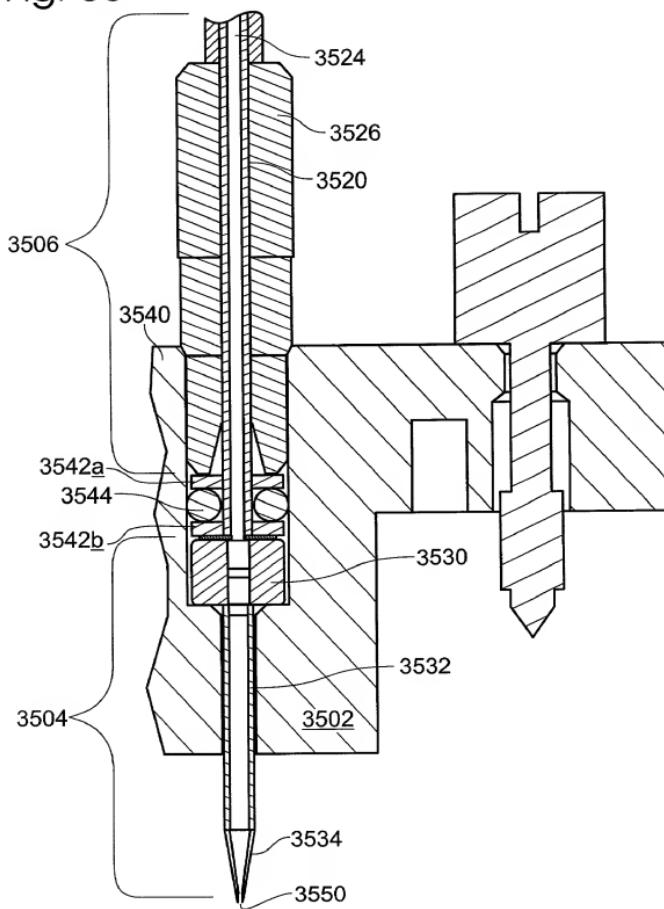


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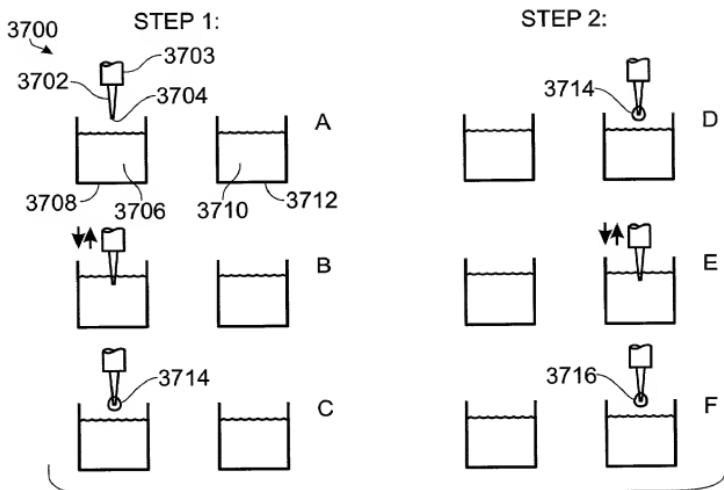


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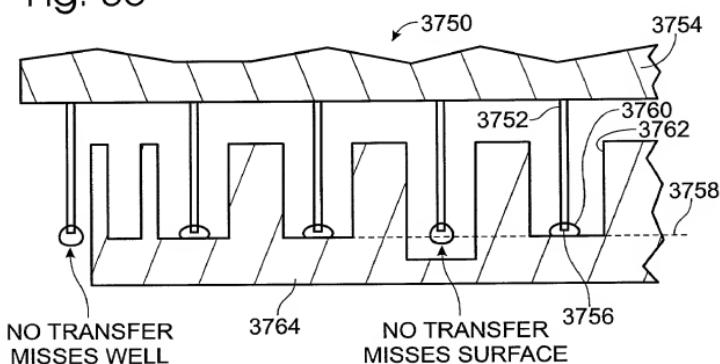


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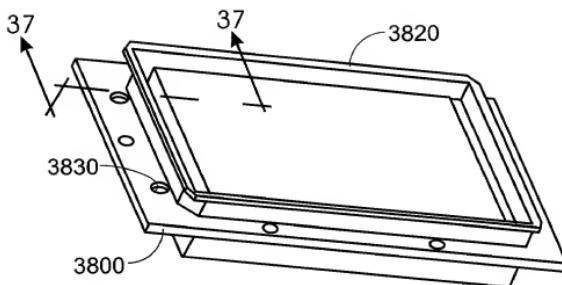


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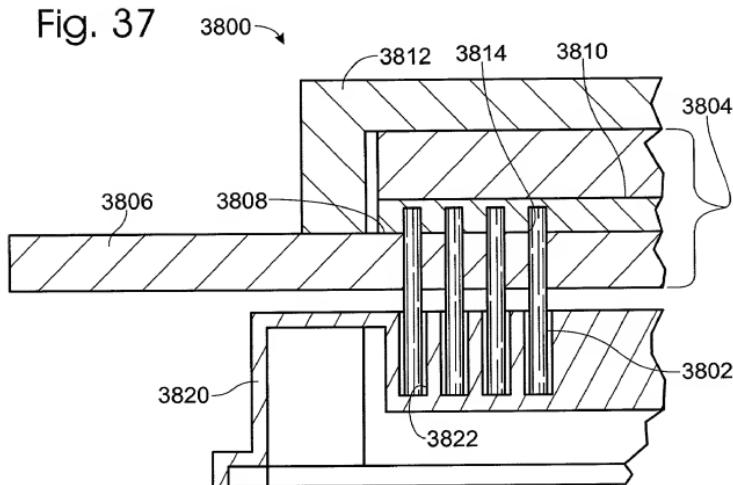


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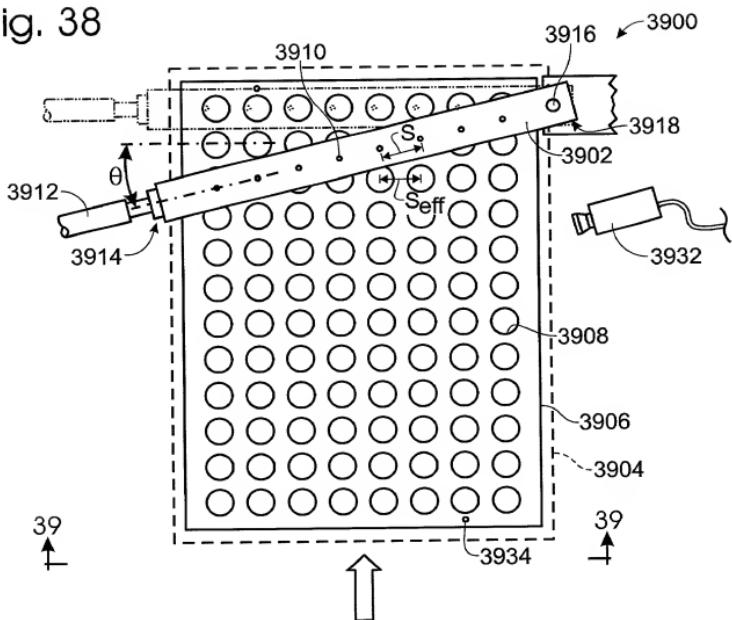


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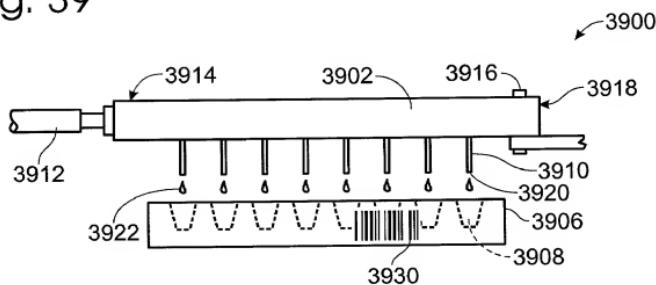
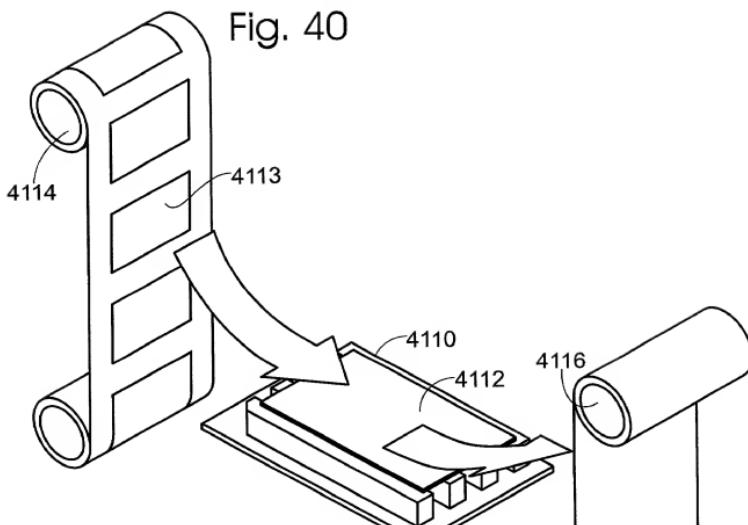


Fig. 40



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Fig. 41

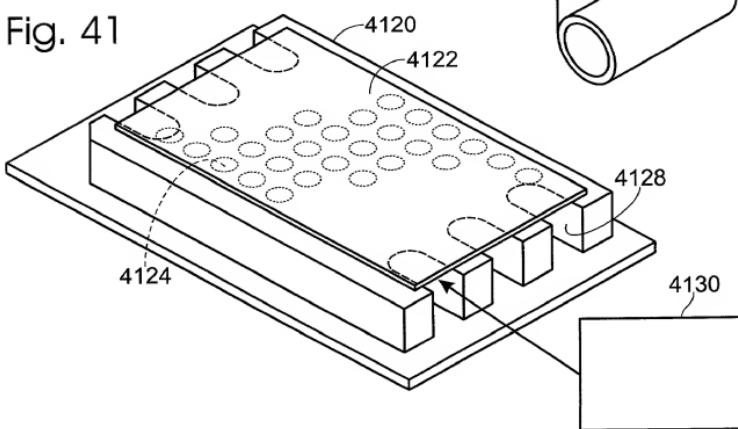


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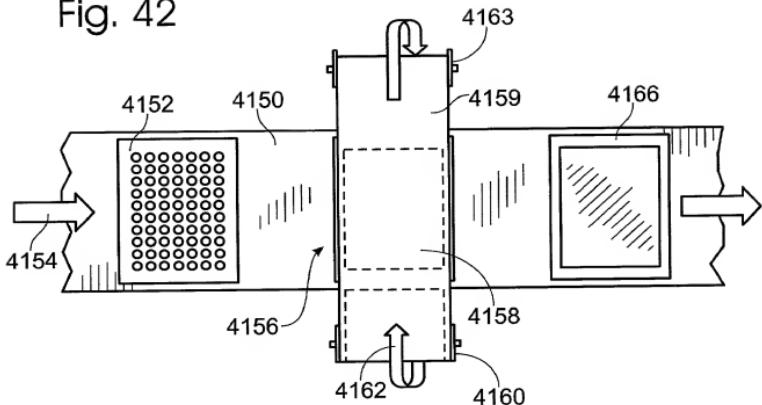


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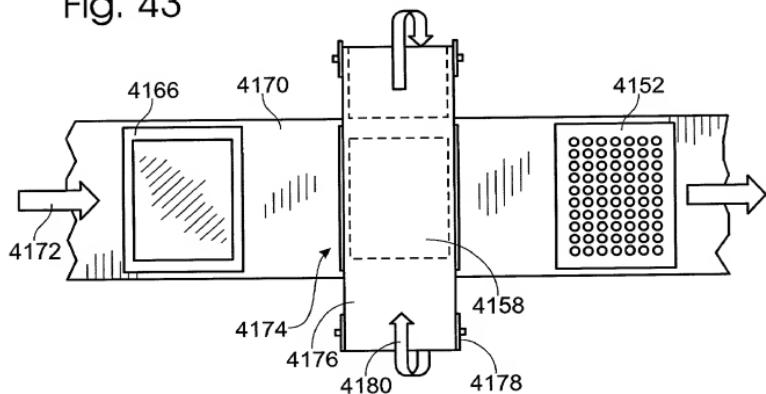


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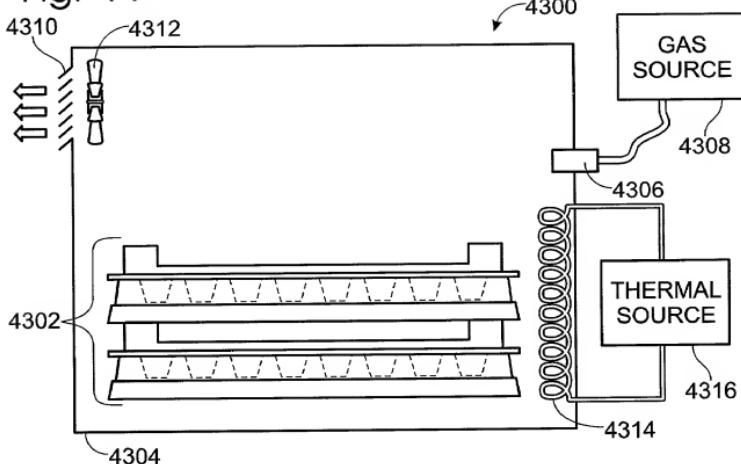


Fig. 45

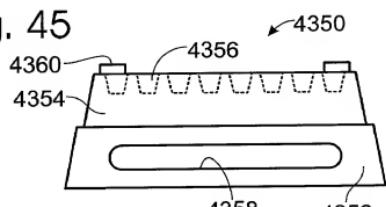


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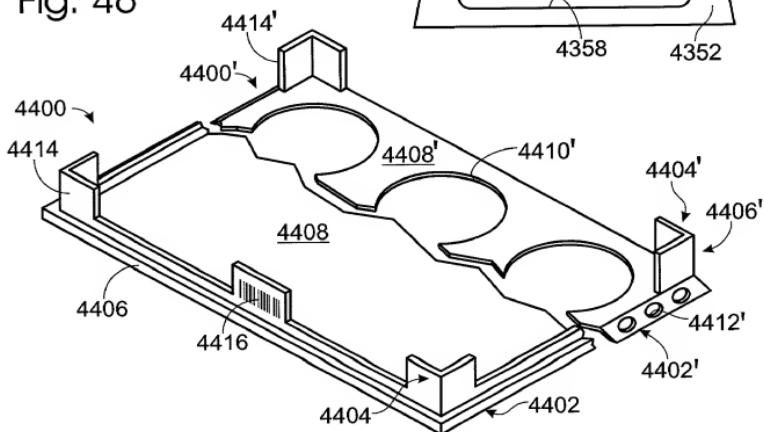


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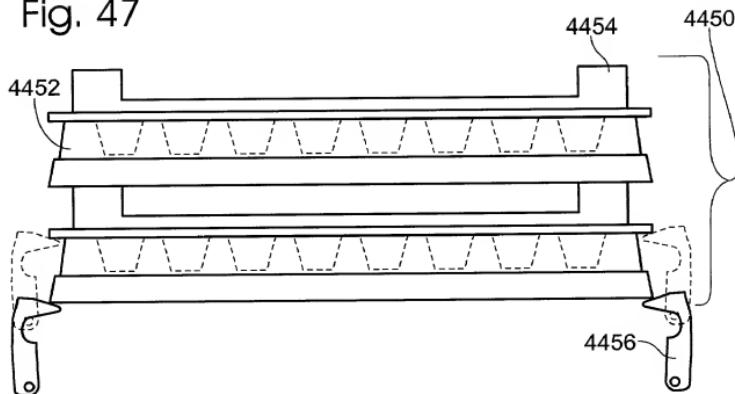
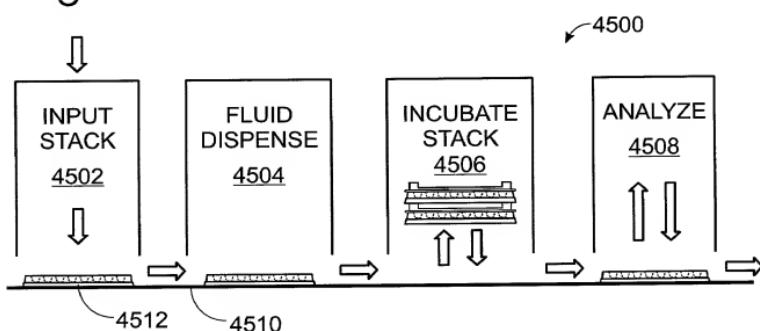
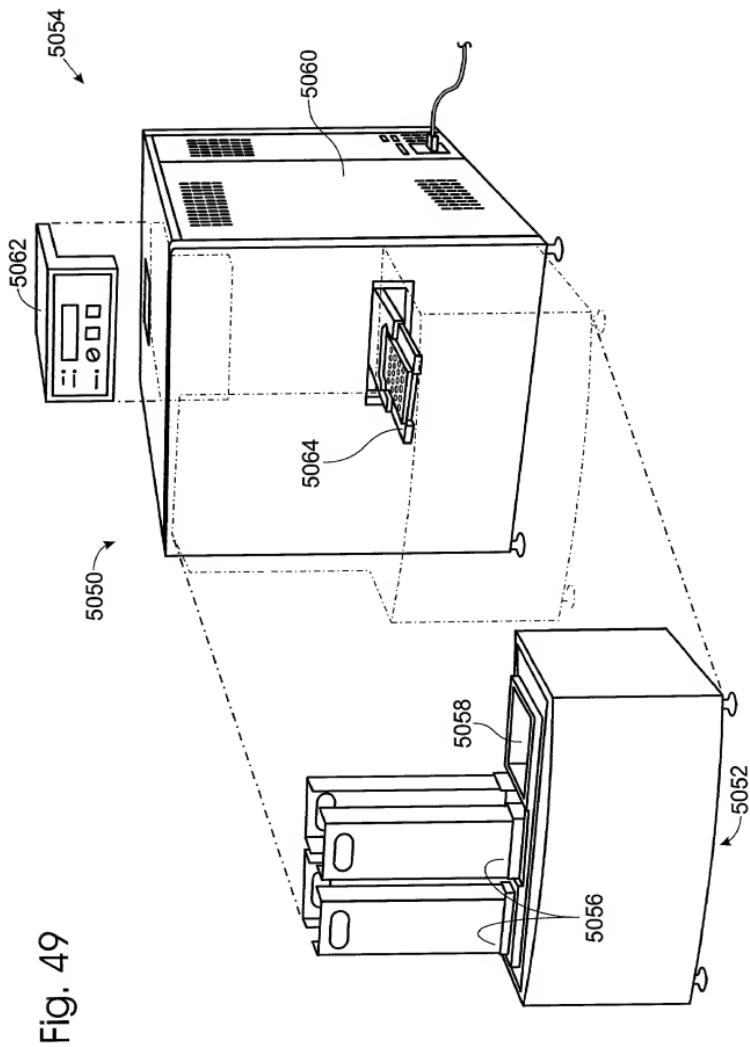


Fig. 48





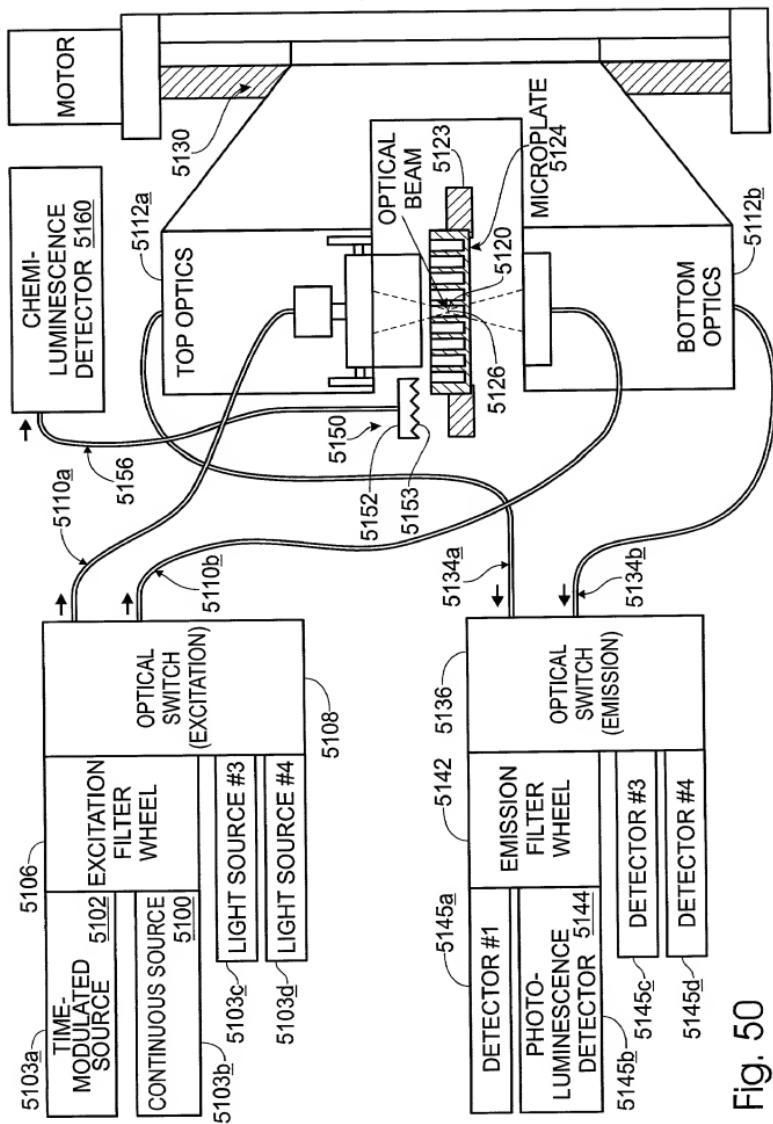


Fig. 50

Fig. 51

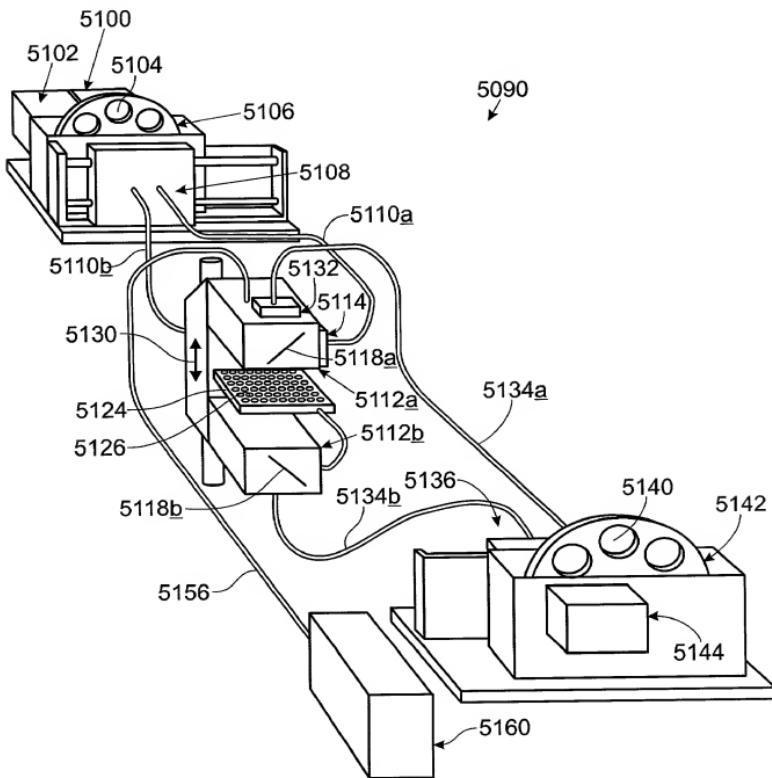


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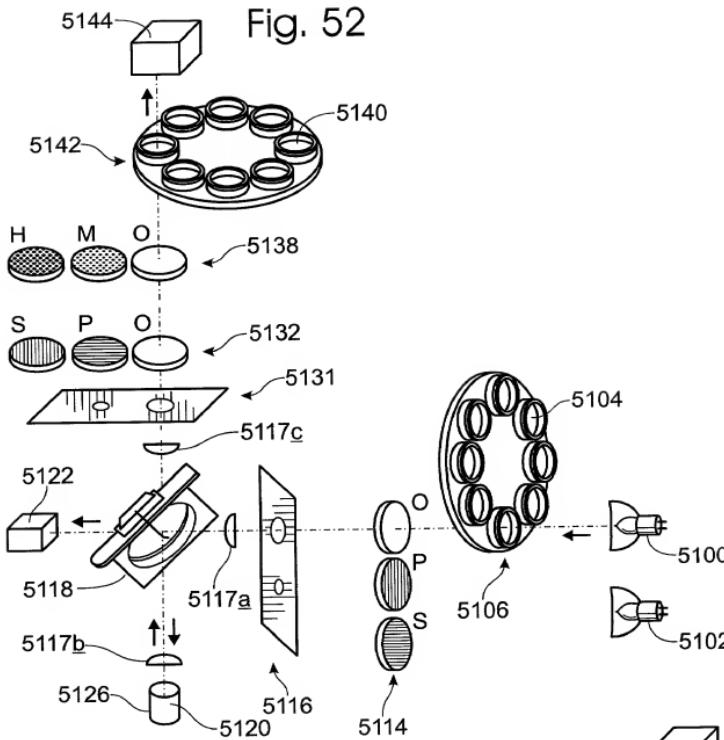


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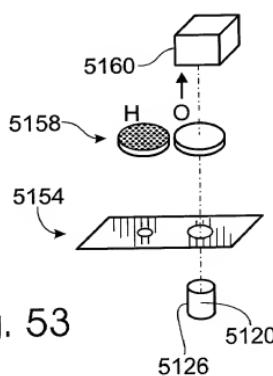


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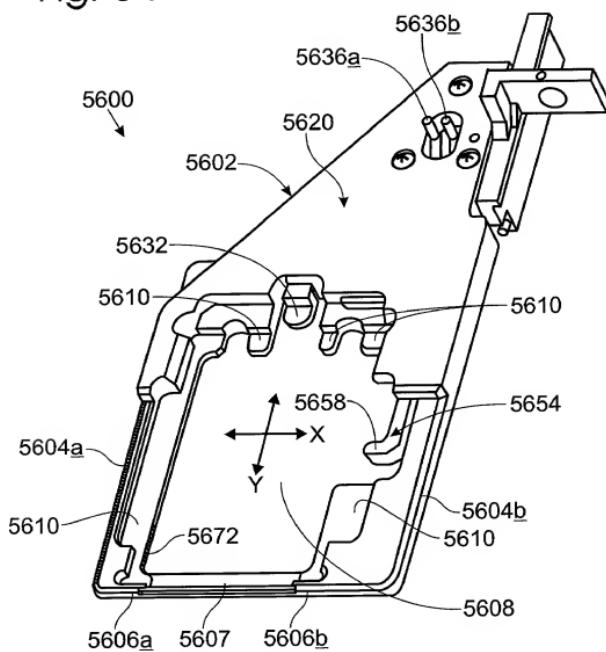


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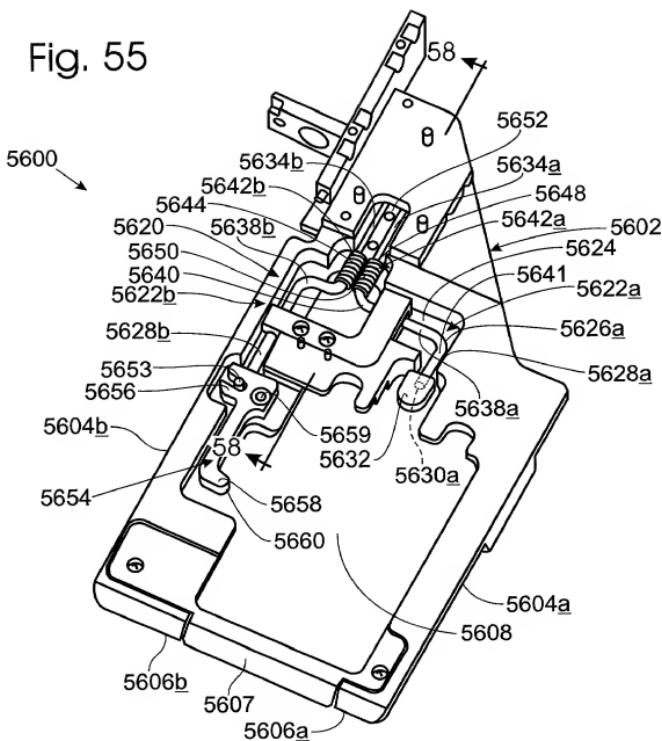


Fig. 56

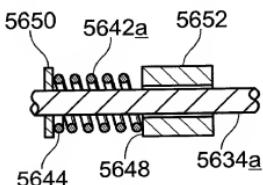


Fig. 57

